Yamaha DA8X Modification from Y2 input to AES input

Modified v3

1. Background:

Yamaha made this DAC with digital signal input using Y2 format with D-SUB 25 female connector of 8 channels audio. It is designed for digital mixing console like DMC1000, DMP7D etc.. Thus it is not able to use for home audio environment as there is no Y2 format digital output source. Yamaha made a FMC9 format converter from AES x 4 to Y2 output via D-Sub 25 socket but is not widely available yet! In order to use it for Home audio, the digital input must be using AES/SPDIF/Toslink sockets but none of these format is build in the DA8X. Why I choose AES input digital format, as far as I know the DA8X use a DIR2 chip YM3436D at its digital input which is same as the Yamaha D2040 digital crossover. By reviewing the service manuals, it is possible to modify the digital board of DA8X to accept AES format.

2. Major parts in DA8X:

1. DIR2 chip: YM3436D – this is a digital interface chip accept both AES/SPDIF and Y2 format signal widely use in Yamaha products since 1988. It is used in D2040 also.
2. YM6067: Parallel to Serial and serial to serial buffer x 2 chips, one chip support total 4 channels digital signal.
3. SM5803APT: 18 or 20 bit 8x oversample filter x 2 chips.
4. PCM63-KY or Y: DAC 20bit x 8 pcs; well know ladder type DAC which sound best back in 1989 period.
5. IV op-amp: M5238 dual op-amp.
6. Drivers op-amp: NE5532.
7. Resistor is 1/8W metal film resistors; not like D2020 use RMA resistors.
8. E-Capacitor: Elna Durex grade, I dissolder and verify the capacitors are still very good after 30 years.
9. Output couple capacitor is MUSE bi-polar Green capacitors.
10. Other film capacitor are either 5% or Soshin brand.

3. Target: Able to use the DAC with such good DAC chips but the digital input must be modified to common SPDIF/AES/Toslink connector. Target is to use AES as the digital board input has a line receiver chip AM26LS32. One for 4 channels data line and one delicate for one channel word clock input sync use. After tracing the signal, the work clock input is connected to EXTW input of YM3436 which is next pin to the digital input of DDIN.

4. Y2 format with D-Sub 25 female socket, out of which, also one channel Word Clock using pin 9 (+) and 22 (-). After tracing the path, it is connected to YM3436 pin 36 EXTW via AM26LS32 line receiver IC5 pin 3. The input pin 1 and 2 of AM26LS32 are connected to the D-Sub 25 pin 9 and 22.

5. The DDIN of YM3436 is pin 37. Thus, first change is to (1) lift up EXTW pin 36, connect to pin 35 CSM which is grounded. So EXTW is now grounded and disable. (2) Then pin 37 DDIN of YM3436 is lift up and connected to the "pad of Pin 36". This is possible as the pin of YM3436D can be straighten and then solder to adjacent pin or adjacent solder pad as shown.

6. YM3436 pin 3 is DOUT signal (decoded from DDIN signal), it is now connected to IC6 YM6067 pin 64 and 62 (3) + (4). Note the Pin 64 and 62 must be lift up from its pad first before connecting to DDIN. There is no trace and thus a jumper wire is used. Use the square PAD next to pin 64 as

support of pin 64, jumper wire to pin 62 and then hot glue all connection to prevent movement. Note that Pin 64 and Pin 62 are the Channel 1-2 and 3-4 digital data input pins. The digital data out from YM6067 is at pin 34 and 36. It is then buffer by HC245 before goes to the connector which use a bus wires connect to DA board. Thus channel 1 is Left channel and channel 2 is R channel at the XLR audio output. Channel 3 is Left channel and channel 4 is Right channels. I did not do for all 8 channels as I think one DA board with 4 channels for me is good enough. Also there is no buffer from DOUT and I worry the driving voltage may be not enough for 4 input pins at YM6067.

7. YM3436 pin 32 is KM0 at High, it must be connected to Low (ground) to select DDIN signal. Thus (5) lift up Pin 32 and then connected to pin 31 KM2 which is connected to Ground.

31	KM2	I	Clock mode select 2 ('H': PLL synchronized, 'L': XI synchronized)
32	KM0	I	Clock mode select 0 ('H': EXTW input, 'L': DDIN input)

8. YM3436 pin 18 DIM1 is at Low (ground), it is required for both DIM1 and DIM0 at High, thus (6) connect the lift pin 18 to pin 17 to high +5V of YM3436.

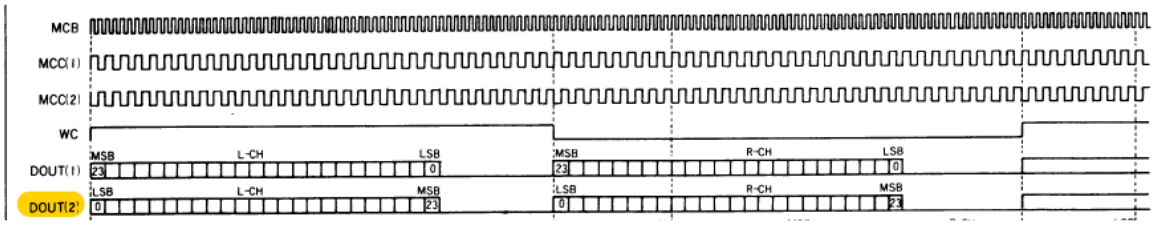
(1) Auxiliary input format

DIM 1	DIM 0	Format
L	L	DAUX(1)
L	H	DAUX(2)
H	L	DAUX(3)
H	H	DDIN input

9. YM3436 DOM1 and DOM0: Default is **High Low**. Change to **Low High**. (7) Lift up pin 21 DOM0 and connect to Pin 22 KM1 which is at HIGH (+5V). (8) Also lift up pin 20 DOM1 and connect to the "PAD of Pin 21" which is at Low (ground). Serial data is reversed as the YM6067 will **reverse** it again!

(2) Data output format

DOM 1	DOM 0	Format
L	L	MCC(1), DOUT(1)
L	H	MCC(1), DOUT(2)
H	L	MCC(2), DOUT(3)
H	H	MCC(1), DOUT(4)



10. AES input connection:

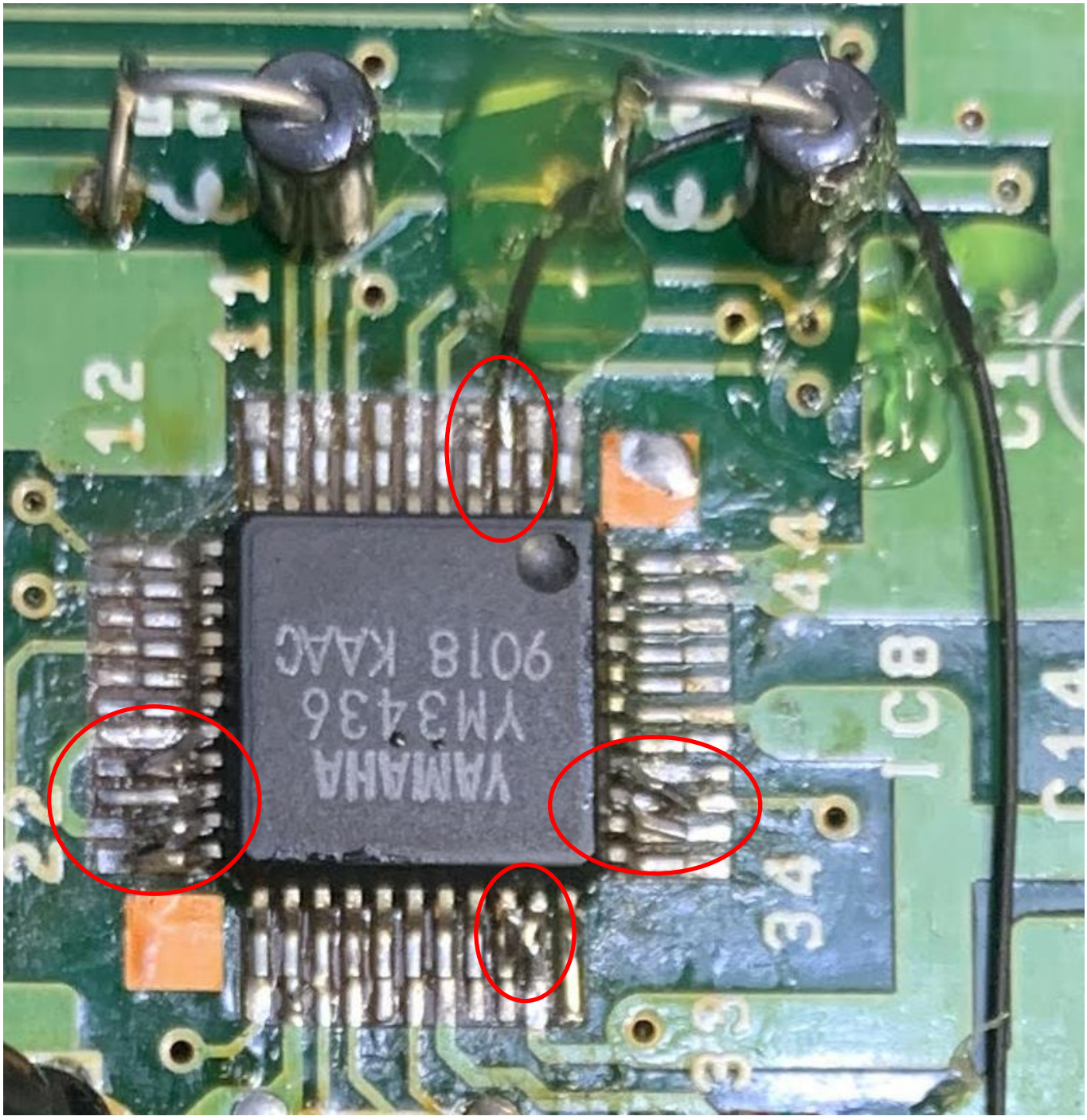
Pin 9 and Pin 22 of D-SUB 25 socket. In fact, a female XLR connector can be install to the back of chassis and connect as below. Pin 9 connect to pin 2 of XLR, Pin 22 connect to pin 3 of XLR. The pin 1 on XLR connected to the ground plan of the D-sub 25 PCB.

11. Audio Signal output:

Output Channel	Left Channel	Right Channel
Group 1	1	2
Group 2	3	4

Other information:

1. YM6067 pins
2. Y2 format pin
3. D-Sub Y2 pin
4. Photo of modified set
5. YM3436 datasheet
6. Draft notes



1. **YM6067 pins:**

In fact, this chip is NOT needed if the Y2 format choose to use MSB first in the digital Data pin. The only function of the YM6067 is to reverse (pin 40 ECCO is High) the LSB first to MSB first data stream in this DA8X because PCM63 accept digital data with MSB first. Thus, I also need to modify the YM3436 to output LSB first data stream in this modification.

• YM6067 (XH494A00) PSC4 (Parallel Serial Converter)

MAIN: IC159

PIN NO.	NAME	I/O	FUNCTION
1	D23	I/O	Parallel I/O ports (D00: LSB, D23: MSB)
2	D22	I/O	
3	D21	I/O	
4	D20	I/O	
5	D19	I/O	
6	D18	I/O	
7	D17	I/O	
8	D16	I/O	
9	D15	I/O	
10	Vss		Ground
11	D14	I/O	Parallel I/O ports (D00: LSB, D23: MSB)
12	D13	I/O	
13	D12	I/O	
14	D11	I/O	
15	D10	I/O	
16	D09	I/O	
17	D08	I/O	
18	D07	I/O	
19	D06	I/O	
20	D05	I/O	
21	D04	I/O	
22	D03	I/O	
23	D02	I/O	
24	D01	I/O	
25	D00	I/O	
26	VDD		Power supply
27	Vss		Ground
28	OENP	I	Output control terminal for parallel ports D00-D15. When Lo: internal bus → external When BA0 is Hi, the impedance of the parallel ports will be Hi even if this is set to Lo.
29	BA0	I	Terminal for selecting origin of data writing for the serial output section. When Lo: serial input section → serial output section. When Hi: parallel port → serial output section However, control cannot be carried out except when MODA=MODB=Lo.
30	MODA	I	4 Internal Blocks
31	MODB	I	1: Serial Input section (SI) 2: Serial Output section (SO) 3: Buffering section (BUF) 4: Parallel port section (PARA) Terminals used to determine how connections are made.

MODB	MODA	Signal Path	AI0, 1:A00, 1: BAO: WTN
0	0	SI → SO PARA	Enabled
0	1	SI → SO PARA	Disabled
1	0	SI → BUF → SO PARA	Disabled
1	1	SI → BUF → SO PARA	Disabled

PIN NO.	NAME	I/O	FUNCTION
			The input and output channels are the same except when MODA=MODB=Lo.
32	OENO	I	Output control terminal. Works in conjunction with the serial output terminals SO0-3. Output is 0 when Hi, and operation is normal when Lo.
33	SO3	O	Serial data output terminals.
34	SO2	O	
35	SO1	O	
36	SO0	O	

	YAMAHA 24-1	YAMAHA 24-2	YAMAHA 48	YAMAHA 96
SO0	ch 0	ch 0	ch 0, 1	ch 0, 1, 2, 3
SO1	ch 1	ch 1	x	x
SO2	ch 2	ch 2	ch 2, 3	x
SO3	ch 3	ch 3	x	x

PIN NO.	NAME	I/O	FUNCTION
37	AO1	I	Writing channel selection terminals for internal parallel bus → serial output latch. Control cannot be carried out unless MODA=MODB=Lo.
38	AO0	I	
39	WIN	I	Write signal to internal parallel bus → serial output latch. Parallel bus data can be received in the shift out latch when Hi → Lo → Hi. However, control cannot be carried out unless MODA=MODB=Lo.

AO1	AO0	channel
0	0	0
0	1	1
1	0	2
1	1	3

PIN NO.	NAME	I/O	FUNCTION
40	ECCO	I	MSB/LSB reverse control terminal for internal parallel busÂ®serial output. Basic format is maintained when Lo. When this goes Hi, the MSB/LSB are reversed.
41	CO1	I	Serial output selection terminal
42	Vss		Ground
43	CO0	I	Serial output selection terminal

CO1	CO0	FORMAT
0	0	YAMAHA 24-1 (1 channel/1 line)
0	1	YAMAHA 24-2 (1 channel/1 line)
1	0	YAMAHA 48 (2 channel/1 line)
1	1	YAMAHA 96 (4 channel/1 line)

PIN NO.	NAME	I/O	FUNCTION
44	BCKO	O	Parallel to serial conversion clock output terminal for serial output section. Normally connected to SCKO.
45	SCKO	I	Parallel to serial conversion clock input terminal for serial output section. Data from SO0-3 is output at the rising edge of the clock. *The start of a word must always be a rising edge.
46	SYNO	I	Sync word input terminal for serial output section. The start of a word is defined as the third rising edge of the MCKO after going from Hi to Lo.
47	MCKO	I	Master clock input terminal for serial output section. Receives 128 x fs (rising edge first) clock.
48	TST	I	Pin for LSI testing. Normally fixed at Lo
49	RESN	I	System reset terminal
50	MCKI	I	Master clock input terminal for serial input section. Receives 128 x fs (rising edge first) clock.
51	SYNI	I	Sync word input terminal for serial input section. The start of a word is defined as the third rising edge of the MCKI after going from Hi to Lo.
52	SCKI	I	Serial to parallel conversion clock input terminal for serial input section. Data from SI0-3 is received at the falling edge of the clock. Normally connected to BCKI.
53	BCKI	O	Serial to parallel conversion clock output terminal for serial input section. Normally connected to SCKI.
54	CI1	I	Serial input format selection terminals
55	CI0	I	

CI1	CI0	FORMAT
0	0	YAMAHA 24-1 (1 channel/1 line)
0	1	YAMAHA 24-2 (1 channel/1 line)
1	0	YAMAHA 48 (2 channel/1 line)
1	1	YAMAHA 96 (4 channel/1 line)

*Caution is advised when changing modes dynamically. (CI0 and CI1 are latched at the start of a word.)

PIN NO.	NAME	I/O	FUNCTION
56	EXCI	I	MSB/LSB reserve control terminal for serial input → internal parallel bus. Basic format is maintained when Lo. When this goes Hi, the MSB/LSB are reversed.
		I	
		I	
57	Vss	I	Ground
58	VDD	I	Power supply
59	AI1		Register channel selection terminals for serial input → internal parallel bus output. However, control cannot be carried out unless MODA=MODB=Lo. When MODA =MODB=Lo, each word is output 1/4 at a time from channels 0, 1, 2, and 3.
60	AI0		
61	SI3	I	Serial data input terminals.
62	SI2	I	
63	SI1	I	
64	SI0	I	

AI1	AI0	channel
0	0	0
0	1	1
1	0	2
1	1	3

	YAMAHA 24-1	YAMAHA 24-2	YAMAHA 48	YAMAHA 96
SI0	ch 0	ch 0	ch 0, 1	ch 0, 1, 2, 3
SI1	ch 1	ch 1	x	x
SI2	ch 2	ch 2	ch 2, 3	x
SI3	ch 3	ch 3	x	x

2. Yamaha Y2 format:

Pin-outs

1 WCLK +
2 GND
3 Audio data –
4 WCLK –
5 Audio data +
6 20 µH coil to GND
7 20 µH coil to GND
8 GND (in), ENABLE (out)

Figure 4.35 Pinouts of the Yamaha two-channel cascade interface.

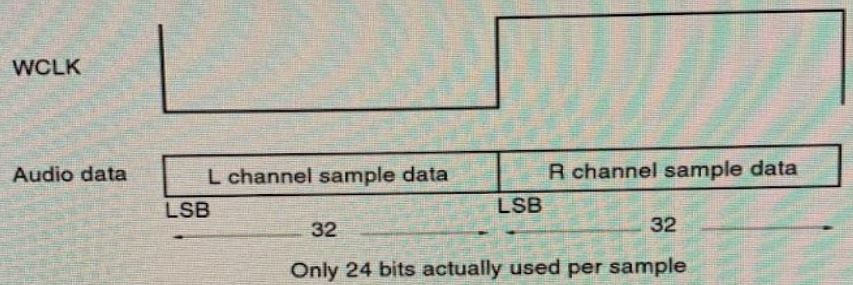


Figure 4.36 Data format of the Yamaha 'cascade' interface.

The two-channel cascade interface terminates in an eight pin DIN-type connector, as shown in Figure 4.35, and carries two channels of 24-bit audio data over an RS-422-standard differential line. The two channels of data are multiplexed over a single serial link, with a 32-bit word of left channel data followed by a 32-bit word of right channel data (the 24 bits of audio are sent LSB first, followed by eight zeros). The word clock alternates between low state for the left channel and high state for the right channel, as shown in Figure 4.36. Coils of 20 µH are connected between pins 6 and 7 and ground to enable suppression of radio frequency interference. The OUT socket is only enabled when its pin 8 is connected to ground.

References

1. AES, *AES3-1985 (ANSI S4.40-1985). Serial transmission format for linearly represented digital*

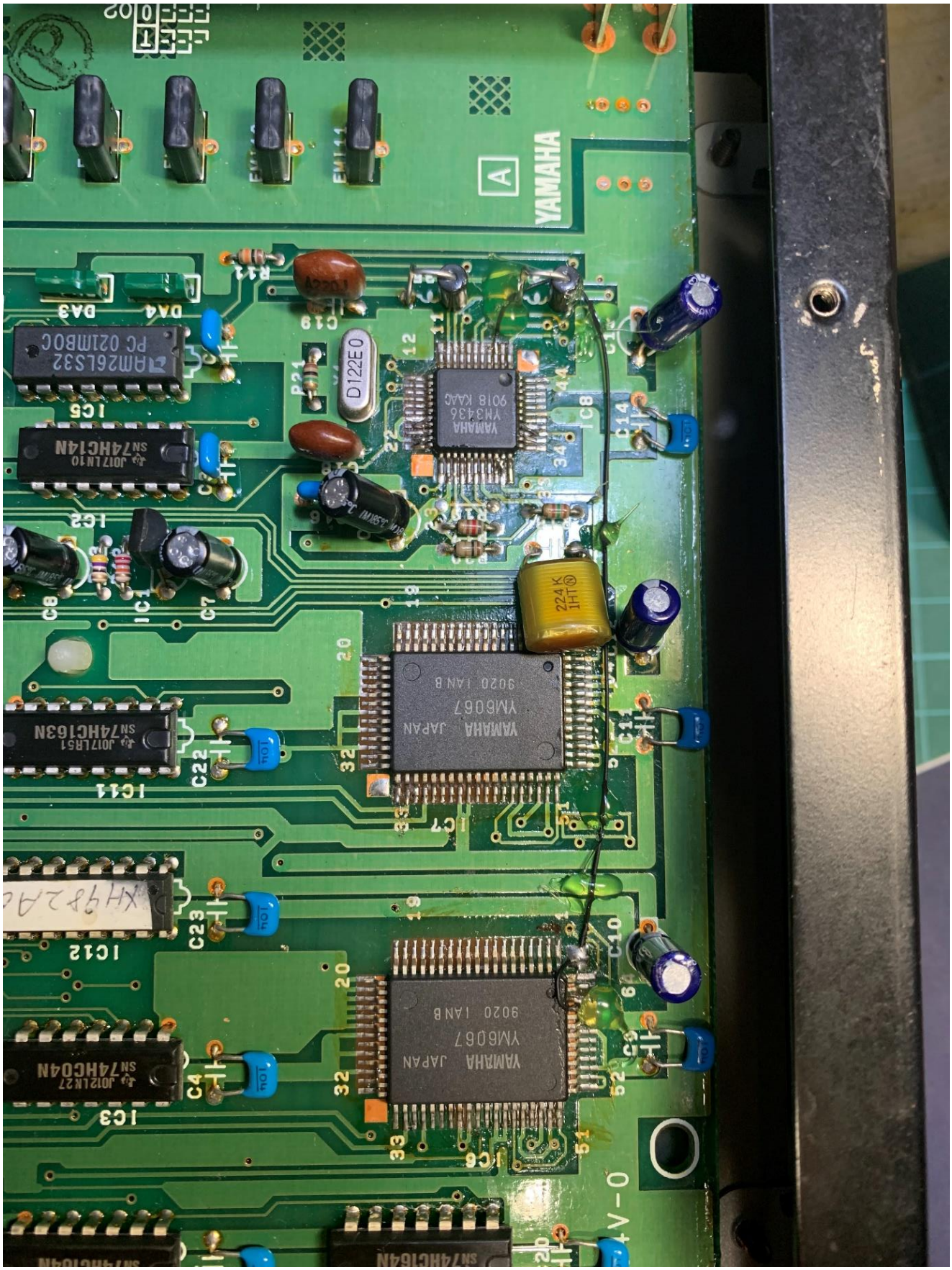
3. **D-SUB25 pins:**

■ Digital Output

PIN No.	Y1	Y2
1	Data CH 1, 2 OUT (+)	Data CH 1, 2 OUT (+)
2	Data CH 2, 1 OUT (+)	Data CH 3, 4 OUT (+)
3	Data CH 3, 4 OUT (+)	Data CH 5, 6 OUT (+)
4	Data CH 4, 3 OUT (+)	Data CH 7, 8 OUT (+)
5	Data CH 5, 6 OUT (+)	N/C
6	Data CH 6, 5 OUT (+)	N/C
7	Data CH 7, 8 OUT (+)	N/C
8	Data CH 8, 7 OUT (+)	N/C
9	Word Clock OUT (+)	Word Clock OUT (+)
10	Word Clock IN (+) *	Word Clock IN (+) *
11	N/C	Emphasis
12	Emphasis	N/C
13	Ground	Ground
14	Data CH 1, 2 OUT (–)	Data CH 1, 2 OUT (–)
15	Data CH 2, 1 OUT (–)	Data CH 3, 4 OUT (–)
16	Data CH 3, 4 OUT (–)	Data CH 5, 6 OUT (–)
17	Data CH 4, 3 OUT (–)	Data CH 7, 8 OUT (–)
18	Data CH 5, 6 OUT (–)	N/C
19	Data CH 6, 5 OUT (–)	N/C
20	Data CH 7, 8 OUT (–)	N/C
21	Data CH 8, 7 OUT (–)	N/C
22	Word Clock OUT (–)	Word Clock OUT (–)
23	Word Clock IN (–) *	Word Clock IN (–) *
24	Ground	Ground
25	Ground	Ground
CASE	Frame Ground	

* Not used by the FMC9.
N/C : No Connection.

4. **Photo of modified set:**

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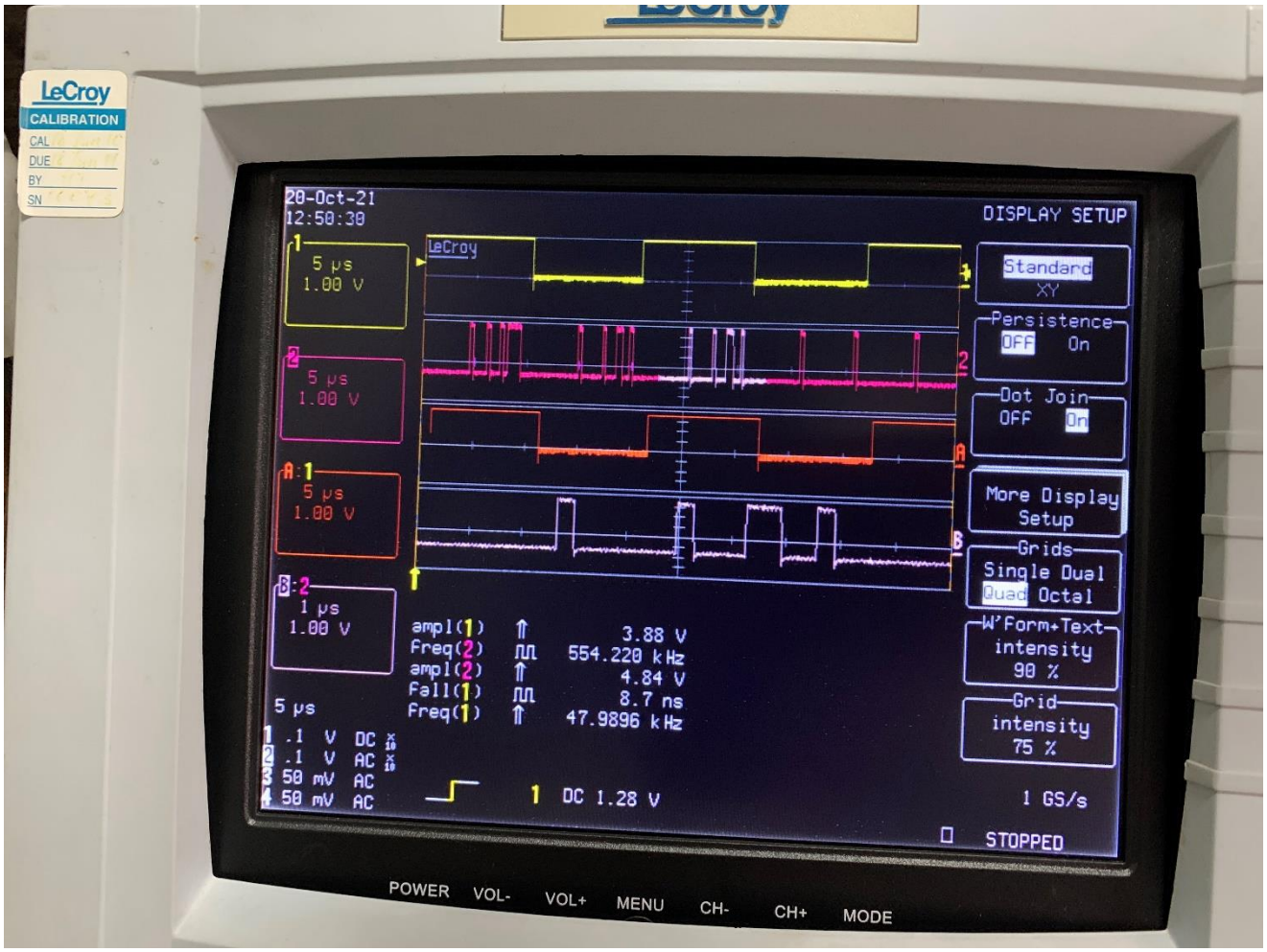
Scope show CN501 work clock pin 1 and data lines pin 2 and pin 5.



5. YM3436 Datasheet:

YM3436.pdf

6. Draft Notes:

DA8X draft notes.pdf

Enjoy Music!

Spencer Cheung

Date: Oct 28, 2021 (V3)